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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,654	09/29/2003	Chun-Chieh Chen	TOP 330	9025

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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,654	CHEN ET AL.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Output node "525" is not labeled on Fig. 5, although it is clearly identified on pages 14 (line 13) and 15 (lines 13, 23, 25 and 30). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 12, lines 26-28 need clarification. These lines imply that Fig. 4 shows the invention's turn-on time is half the turn-on time of the prior art. However, Fig. 4 appears to show the invention's changes in current occur at substantially the same time as the prior art. Therefore, how do these changes relate to the turn-on times as described? Page 15, line 20 "M35 and M37" should be --M55 and M57--to clearly identify the transistors shown in Fig. 5. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

Claims 4-7, 12-15, and 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not understood if each of the first/second cascode current mirrors recited within each of claims 4, 12, and 19 is a wide-swing cascode current mirror, or if the wide-swing cascode current mirror is made up of both the first/second cascode current mirrors. The use of "coupled between" on lines 3, 6, 10, and 13 of each of claims 5 and 13 is misleading. For example, and using the applicants' own Fig. 3 as a reference, the presently worded limitations on lines 3-5 of claim 5 appear to imply that first input mirror transistor M32 is coupled between the (source of) first output mirror transistor M34 and ground. However, was --coupled to-- meant instead of "coupled between"? The phrase --coupled to-- would be accurate, and would also minimize possible confusion with respect to how "between" can be interpreted.

Claim 13 recites the limitations "the first reference current source" and "the second reference current source" in lines 7-8 and 14-15, respectively. There is insufficient antecedent basis for these limitations in the claim. For example, do claim 13's first/second reference current sources make up the single "reference current source" recited in claim 8, line 3?

Note: Depending on how the antecedent problem of claim 13 is addressed, the first/ second reference current sources recited within claim 15 may also need to be changed.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-14, and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeyabu et al. (Takeyabu). Fig. 16 shows a high-speed low-noise charge pump comprising first cascode current mirror NT11-NT13,NT15 coupled to first reference current source 121 and adapted to generate a first mirror current (unlabeled but understood as being applied to the output node between PT15 and NT13 when the first cascode current mirror's output current flows), wherein the first cascode current mirror includes first output mirror transistor NT15 and first output cascode transistor NT13; second cascode current mirror PT11-PT13,PT15 coupled to second reference current source NT16-NT17 and adapted to generate a second mirror current (unlabeled but understood as being applied to the output node when the second cascode current mirror's output current flows), wherein the second cascode current mirror includes second output mirror transistor PT13, and second output cascode transistor PT15 coupled to first output cascode transistor NT13 at the output node; first switching transistor NT14 being turned on during assertion (i.e. high) of a first control signal (output Q of 126) to cause the first mirror current to flow; and second switching transistor PT14 being turned on during assertion (i.e. low) of second control signal (output Q of 126) to cause the second mirror current to flow. Since the source, drain, and gate of first switching transistor NT14 are coupled to first output mirror transistor NT15, first output cascode transistor NT13, and the first control signal, respectively,

and the source, drain, and gate of second switching transistor PT14 are coupled to second output mirror transistor PT13, second output cascode transistor PT15, and the second control signal, respectively, claim 1 is anticipated. NT13-NT15 are n-channel MOS transistors, and PT13-PT15 are p-channel MOS transistors, thus anticipating claim 2. The source and drain connections of transistors NT13-NT15, and PT13-PT15 are clearly shown in Fig. 16, and understood by one of ordinary skill in the art. Therefore, claim 3 is also anticipated. The combination of the first/second cascode current mirrors is deemed a wide swing cascode current mirror because they allow the voltage provided at the output node to substantially range between the (positive) voltage supply and the (low) voltage supply (e.g. ground), anticipating claim 4. The first cascode current mirror further comprises first input mirror transistor NT12 coupled to first output mirror transistor NT15 and ground, and a first input cascode transistor NT11 coupled to first output cascode transistor NT13 and first reference current source 121; and the second cascode current mirror further comprises second input mirror PT11 coupled to second output mirror transistor PT13 and the voltage supply, and second input cascode transistor PT12 coupled to second output cascode transistor PT15 and second reference current source NT16-NT17 to anticipate claim 5. NT11-NT12 are n-channel MOS transistors, and PT11-PT12 are p-channel MOS transistors, anticipating claim 6. Interpreting Fig. 16 in a slightly different manner, reference current source 121 provides a supply current directly to first cascode current mirror NT11-NT13,NT15, and effectively (e.g. indirectly) provides the supply current to second cascode current mirror PT11-PT13,PT15. Therefore, reference current source 121 is considered as being coupled to the first/second cascode current mirrors, and claims 8-14 are anticipated for the same type of reasoning as applied to claims 1-6 as previously described. With similar

reasoning, but in yet another interpretation of Fig. 16, first switching transistor NT14 has its source, drain, and gate coupled to the drain of first output mirror transistor NT15, the source of first output cascode transistor NT13, and first control signal, respectively, and second switching transistor PT14 receives a second control signal to cause the second mirror current from second cascode current mirror PT11-PT13,PT15 to flow. Since NT13 and NT15 are included within first cascode current mirror NT11-NT13,NT15, claims 16-19 are anticipated for the same reasoning as applied to previous, corresponding claims (e.g. see claims 3-4).

No claim is allowable.

Allowable Subject Matter

However, claims 7, 15, and 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. [Note: The rejection may be carried over from a claim upon which the dependent claim depends upon.] There is presently no strong motivation to modify or combine any prior art reference to ensure the input cascode transistor is coupled (e.g. its drain is coupled to the gate of the corresponding input mirror transistor) as recited within claims 7 (lines 7-9 and 15-17), 15 (lines 7-9 and 15-17), and 20 (lines 8-10).

Prior Art

The other prior art reference(s) cited on the accompanying PTO-892 are deemed relevant to most of the claimed limitations. Although not used in any formal rejections described above, each of these references could have been used to reject claims for the same type of reasoning as described above with respect to the Takeyabu et al. reference, and/or an obvious modification

could be made to each reference to read on the claimed limitations. Fig. 6 of Yang shows first cascode current mirror N57,N51,N58,N52, first reference current source 53, first switching transistor N53, first control signal DN, second cascode current mirror P51,P57,P52,P58, second reference current source 51, second switching transistor P53, and second control signal /UP. The reference teaches the cascode arrangement is used when increased output impedance is required (e.g. see column 8, lines 50-52). Although switching transistors P53 and N53 are not shown coupled between their corresponding output mirror transistor and output cascode transistor, it would have been obvious to change them to that position for at least one of two reasons: 1) with the switching transistor placed between the other two transistors, the switching transistor would be isolated from both its supply voltage and the output node; and 2) as long as the switching transistor is still coupled in series with the other two transistors, control of the switching transistor would still allow control of the current flow through those transistors. Also, even though two separate current sources are shown in Fig. 6, if they both provide the same amount of current, it would be obvious to one of ordinary skill in the art that the two current sources could be replaced by a single current source providing the same current to each of the first/second cascode current mirrors. Fig. 2 of Warner shows first/second cascode current mirrors 76,78,62,64/74,72,60,58, first/second switching transistors 54/52, first/second control signals N/P, and reference current source 68,66,70. For the same reasoning as described above with respect to the Yang reference, the series connection of the switching transistors could be changed with respect to the output mirror transistor and output cascode transistor. This reference also teaches the use of cascode stages provides "excellent linearity and current control" (e.g. see column 5, lines 1-3). Desbonnets' Fig. 1 does not clearly show first/second cascode current

mirrors, but does show cascode arrangements with respect to current mirrors (e.g. see PM1-PM2,PM4-PM6), wherein a switching transistor (e.g. see PM3) is coupled between an output mirror transistor (e.g. PM2) and an output cascode transistor (e.g. see PM4 and/or PM6). Also, the reference clearly discloses PM6 and NM6 are related to "cascoded current mirrors...well-known to any person skilled in the art and not shown" (e.g. see column 6, lines 14-19). The reference of Rhee et al., described in the disclosure and cited here to ensure it will be identified on the front page if/when the application is allowed, discloses cascode circuits reduce switch noise and switching time (e.g. see column 1, lines 9-10) by isolating the switching transistors from the output (e.g. see column 7, lines 9-10), and the cascode circuits also increase output impedance (e.g. see column 9, lines 59-61), thus improving the output voltage range. Also, Rhee et al. discloses the cascode circuits could employ more transistors, and additional transistor stages could be added (e.g. see column 7, lines 11-15). Therefore, one of ordinary skill in the art would understand the circuit could use cascaded current mirror arrangement. All of the above references should be carefully reviewed and considered with respect to the claim limitations recited within the application's broadest claims.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund

6 December 2004

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